# Non-Ideality Analysis of Clock-Jitter Suppressing Sampler for Wideband ΣΔ Analog-to-Digital Converters

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*Abstract* — **As CMOS processes evolve into smaller and smaller feature sizes, the ability to clock circuits at higher rates and the need of integrating analog and digital systems on a single chip arises. This makes it suitable to use a wideband ΣΔ Analog-to-Digital Converter (ADC), due to its high digital content and robustness against circuit imperfections, as part of a front end for a 3rd or 4th generation mobile communications system. One type of ΣΔ that would be appropriate for such an application is suggested in [1]. However, wideband operation sets tough jitter constraints on the clock since the oversampling ratio (OSR) is lower than for traditional ΣΔ ADCs. Previously [2], we have proposed a sampling circuit topology which helps to reduce the effects of non-uniform sampling by averaging. This topology's jitter suppressing properties are based on certain assumptions which, in reality, are non-ideal. This paper describes an analysis of those non-idealities and their impact on the topology's jitter suppressing features on a circuit level.**

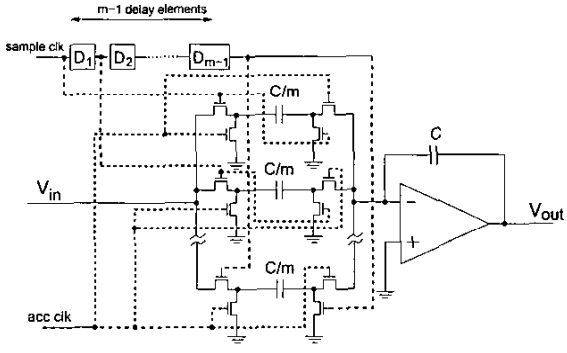


Fig. 1. Single-ended version of previously proposed SC sampling circuit ΣΔ front-end.

## I. Introduction

When the sample rate of an analog signal is only one order of magnitude higher than the signal bandwidth, clock jitter issues become important [3]. Therefore it is paramount to use a clock with low jitter. However, if no such clock is available it is necessary to investigate what can be done with a jittery clock to improve the ADC resolution.

Previously [4] we, and others to some extent [5], [6], have analyzed the effects of clock jitter in SC ΣΔ ADCs. This analysis shows that non-uniform sampling (NUS) clock jitter has an impact which is roughly proportional to the square of the analog signal's frequency. It also shows that not only the signal's frequency influences the jitter impact but also the order of the ΣΔ and the settling accuracy[1]. However, at higher signal frequencies, with a constant and high settling accuracy, the frequency dependent NUS jitter is the dominant parameter in the jitter impact. To address the problem of NUS clock jitter we have presented [2] a SC front-end topology for wideband ΣΔs which attempts to reduce the effects of a jittery clock (see Fig. 1). A pipeline of $m-1$ delay elements form a delay line where each element delays the sampling clock by one clock cycle. After the first $m-1$ clock cycles, the pipeline is full and the input signal is sampled $m$ times in parallel for each clock cycle. If jitter on different clock-edges are independent, the total error is reduced, as compared to using a standard SC topology, due to averaging. The basis of the proposed topology's success is an assumption of period-to-period clock jitter independence and sample-group independence, i.e. independence within the sample group and also between different sample groups. Further assumptions that have been made previously [2] are ideal delay elements, i.e. no inherent delay-offset, no delay-jitter and no jitter preservation in the delay line. When these assumptions hold, the topology suppresses NUS jitter error power by $10\log(m)$ dB uniformly $\{0 \rightarrow \frac{f_s}{2}\}$, given White-Gaussian-Noise jitter. When the period-to-period clock jitter is fully dependent, no improvement is obtained. In reality, neither full dependence nor full independence is likely but something in-between.

In this work we have analyzed the effects of jitter accumulation in the delay line and investigated how the delay elements' properties affect the total jitter suppressing performance of the proposed sampler. The calculations and simulations in this paper are based on period-to-period jitter independence since information regarding dependence has to be measured on a case-to-case basis. However, sample-

[1] Determines the slope of the settling curve at the end of each sampling phase. Thereof the definition Varying-Phase-Length (VPL) jitter.



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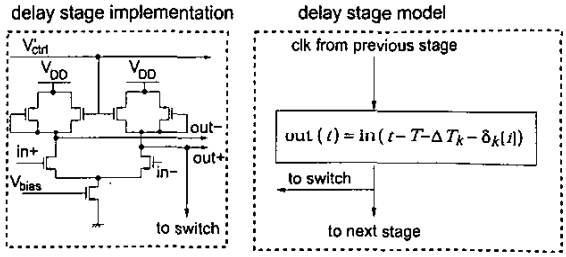


Fig. 2. (a) Example of a delay element implementation and (b) delay element analysis model.

group independence has not been assumed since this is a equivalent of not having jitter preservation.

## II. Delay Line Properties

The delay line from Fig. 1 is the backbone of the jitter suppressing topology. An implementation suggestion [7], [8] is a replica biased delay line. An example of a delay element is shown in Fig. 2a. A replica circuit [8], controlled by $V_{\text{ctrl}}$, adjusts the tail current of each differential delay element in the delay line, through $V_{\text{bias}}$, to make the voltage of the drains of the PMOS transistors equal to $V'_{\text{ctrl}}$. This arrangement assures that the triode connected PMOS transistors, which are equally sized as the diode connected transistors, stay in saturation. Process variations will cause static delay variations $\Delta T_k$ in each delay stage $k$ of the delay line. Power supply noise, especially high frequency noise, will induce jitter $\delta_k[i]$ in the delay line. This jitter is referred to as delay jitter. One way of trying to compensate for this is to employ some sort of supply filtering. A simple method would be to use a low-pass filter between the supply source $V_{\text{DD}}$ and a "clean" supply dedicated to the delay elements if the bandwidth of the replica control loop is high enough.

NUS jitter and VPL jitter are properties of the clock signal as it reaches the delay line. When the clock signal is delayed by the delay elements, delay jitter and static delay errors add to the clock. This additional distortion may affect the statistical dependence of jitter before a delay element and after. Jitter preservation in this sense is important to investigate in order to properly determine the total jitter impact on the proposed topology. To illustrate jitter preservation, consider, for example, the two NUS jitter-groups $\{\gamma_1[i], \gamma_2[i] \ldots, \gamma_m[i]\}$ and $\{\gamma_1[i+1], \gamma_2[i+1] \ldots, \gamma_m[i+1]\}$ which are part of the $m$ clock signals controlling the sampling capacitors in clock cycles $i$ and $i+1$. Previously [2], we have considered jitter not to be preserved through a delay element which means the two sampling groups are fully independent. If the elements within each group are also independent, the averaging property of the sampling structure reduces the standard deviation of the NUS jitter by a factor $m$.

However, if jitter properties are fully preserved through the delay line, the two sample groups are equivalent to $\{\gamma[i], \gamma[i-1] \ldots, \gamma[i-(m-1)]\}$ and $\{\gamma[i+1], \gamma[i] \ldots, \gamma[i-(m-2)]\}$ which are clearly dependent. The dependence stretches $m$ clock cycles which means that as $m$ increases, the suppression performance should get saturated in some sense.

There may also be partial dependence between $\gamma_k[i]$ and $\gamma_{k+a}[i+a]$. However, this case has not been investigated here but should be analyzed through measurements.

## III. Performance Calculations

An expression describing the voltage over the $k^{\text{th}}$ sampling capacitor using the proposed scheme with the non-idealities mentioned above, given full settling, is

$$V_k[i] \approx V_{\text{in}}\left( it_s + \underbrace{\gamma[i-k]}_{\text{(i)}} + \underbrace{\sum_{j=1}^{k} \Delta T_j}_{\text{(ii)}} + \underbrace{\sum_{q=1}^{k} \delta_q[i-(k-q)]}_{\text{(iii)}} \right) \tag{1}$$

where (i) is the NUS jitter, (ii) is the static delay error, and (iii) is the delay jitter as the clock goes through one delay element. Similarly, the change in output voltage is given by the relation

$$\Delta V_{\text{out}}[i] \approx \frac{1}{m} \sum_{k=0}^{m-1} V_k[i] \tag{2}$$

In case the static delay errors $\Delta T_k$ are negligible and $\omega\left(\gamma[i-k] + \sum_{q=1}^{k} \delta_q[i-(k-q)]\right) \ll 1$, $\forall\{i,k\}$, a good approximation to the sampled voltage is

$$V_k[i] \approx V_{\text{in}}[i] + V'_{\text{in}}[i]\left(\gamma[i-k] + \sum_{q=1}^{k} \delta_q[i-(k-q)]\right) \tag{3}$$

To get an estimate of the jitter power spectrum we use (2) and (3) to obtain the stochastic error term $\Delta V_{\text{err}}[i] = \Delta V_{\text{out}}[i] - \Delta V_{\text{out,ideal}}[i]$. Next we form the autocorrelation function

$$r[i,p] = \text{Cov}\{\Delta V_{\text{err}}[i+p], \Delta V_{\text{err}}[i]\} \tag{4}$$

An overestimate of $r[i,p]$ is made, $\hat{r}[p]$, to give weak stationarity which allows us to use the Wiener-Khinchin theorem to obtain an estimate of the jitter power spectrum (JPS).

$$\text{JPS}(f_d) = R(f_d) = \mathcal{F}_{\text{td}}\{\hat{r}[p]\} \tag{5}$$

The result, where $\gamma$ and $\delta$ are assumed to belong to White-Gaussian-Noise (WGN) processes and the analog signal is

$$\mathrm{JPS}(f_d) \le \left(\frac{A\omega}{m}\right)^2 \sum_{p=1}^{2m-2} (\cos(2\pi f_r p)+1)\cos(2\pi f_d p)\left((m-p)\sigma_{\mathrm{NUS}}^2 + \frac{\sigma_d^2}{2}(m-1-p)(m-2-p)\right) +$$
$$+ \left(\frac{A\omega\sigma_{\mathrm{NUS}}}{m}\right)^2 \Big(\cos(2\pi f_r(m-1))+1\Big)\cos(2\pi f_d(m-1)) + \left(\frac{A\omega}{m}\right)^2 \left(m\sigma_{\mathrm{NUS}}^2 + \frac{\sigma_d^2}{2}(m-1)(m-2)\right) \quad (6)$$

$V_{\mathrm{in}}(t) = A\sin(2\pi f_{\mathrm{sig}} t)$, is shown in (6). $\sigma_{\mathrm{NUS}}^2$ is the NUS jitter variance, $\sigma_d^2$ is the delay jitter variance, $\omega = 2\pi f_{\mathrm{sig}}$, $f_r = \frac{f_{\mathrm{sig}}}{f_s}$, and $f_d = \frac{f}{f_s} \in [-\frac{1}{2}, \frac{1}{2}]$.

The previous discussion has not taken $\Delta T_k$ into account. To do that we perform a Nyquist range SNR calculation. Equations (2) and (3) are used as starting point. However, (3) has to be modified slightly.

$$V_{\mathrm{in}}[i] \to V_{\mathrm{in}}\left(it_s + \sum_{j=1}^{k} \Delta T_j\right) \quad (7)$$

Assuming $\omega \sum_{j=1}^{k} \Delta T_j \ll 1$, $\forall k$, we obtain, in a similar way as the previous deduction, an estimate of the Nyquist range error power.

$$P_{\mathrm{noise}} \le \hat{r}[0] \approx (A\omega)^2 \left[\sigma_{\mathrm{NUS}}^2\left(\frac{1}{m} + \left(\frac{\omega}{m}\right)^2 \sum_{p=0}^{m-1} D^2[p]\right) + \right.$$
$$\left. + \frac{\sigma_d^2}{2}\left(1 - \frac{1}{m} + \left(\frac{\omega}{m}\right)^2 \sum_{p=0}^{m-1} pD^2[p]\right)\right] \quad (8)$$

where $D[p] = \sum_{j=1}^{p} \Delta T_j$.

## IV. Simulations

MATLAB simulations have been made with a fourth order 2-2 cascaded $\Sigma\Delta$ topology [9] with two $\infty$-bit quantizers to allow for observations of jitter attributed noise. The NUS jitter, VPL jitter and delay jitter elements have been randomly chosen from independent, zero mean, Gaussian distributions with variances $\sigma_{\mathrm{NUS}}^2, \sigma_{\mathrm{VPL}}^2$, and $\sigma_d^2$ respectively. The input signal amplitude has been 0.1 V with a frequency of 1.125 MHz. Moreover, throughout all simulations, the sampling clock had a duty cycle of 25 %, frequency 96 MHz and an OSR of 16. Static delay errors have been taken from a Gaussian distribution with standard deviation, $\sigma_{\Delta T}$ and zero mean. Phase overlaps have not been considered in simulations because this phenomenon only appears when using high duty-cycle clocks and/or clocks with very poor jitter characteristics and/or a very poor delay line. Neither of these are considered relevant for this analysis.

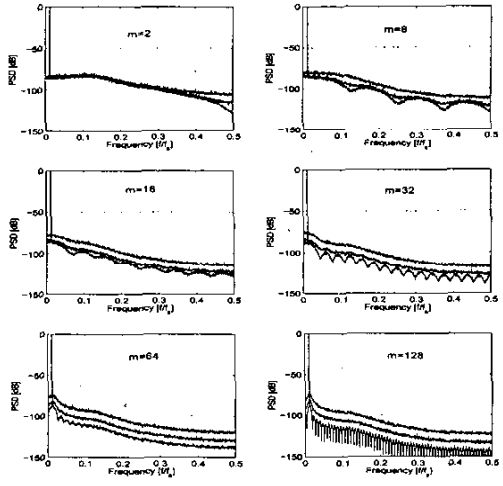


Fig. 3. PSD plot with NUS and delay jitter attributed noise assuming full settling. $f_{\mathrm{sig}} = 1.125$ MHz, $\sigma_{\mathrm{NUS}} = \frac{0.1}{f_s}$ and $\sigma_d = \frac{\{0, 0.03, 0.1\}}{f_s}$.

The plot in Fig. 3 shows the power spectral density (PSD) of the $\Sigma\Delta$ output for different number of input capacitors $m$. This plot clearly shows how the noise becomes more colored as $m$ increases. Moreover, the suppression becomes frequency dependent although the total NUS error power falls as $\frac{1}{m}$.

Further simulation results deal with how the inband SNR is affected by having different numbers of input capacitors versus different amounts of delay jitter and static delay errors. Fig. 4 show that at $\sigma_d \approx 0.3\sigma_{\mathrm{NUS}}$ there is no benefit of using the proposed topology and at even higher $\sigma_d$'s the SNR falls as the number of input capacitors increases.

Fig. 5 shows that varying the static delay errors $\sigma_{\Delta T} = \{0 \to \frac{0.1}{f_s}\}$ has little effect on the theoretical SNR. According to eq. (8), a decay of the delay accuracy will not be a significant factor in itself, in terms of noise impact. However, it is most significant in an indirect way because lower delay accuracy results in higher probability of phase overlap which, in turn, increases the noise considerably. In order to reduce this possibility, a tradeoff has to be made between duty cycle, which influences phase overlap probability, and

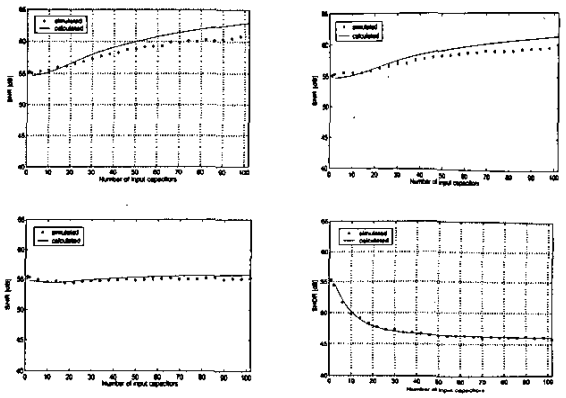

Fig. 4. Plot of inband SNR when $\sigma_d = \{0.01, 0.1, 0.3, 1\}\sigma_{\text{NUS}}$, $\sigma_{\text{NUS}} = \frac{0.1}{f_s}$, $\sigma_{\text{VPL}} = \frac{0.1}{4f_s}$, settling accuracy is 14 bits, and $\sigma_{\Delta T} = \frac{0.01}{f_s}$.

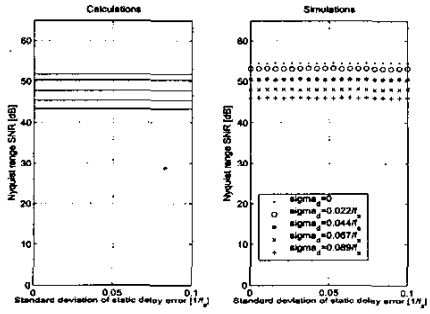


Fig. 5. Plot of SNR when varying the static delay errors for different $\sigma_d$. $\sigma_{\text{NUS}} = \frac{0.1}{f_s}$, $\sigma_{\text{VPL}} = \frac{0.1}{4f_s}$ and settling accuracy is 14 bits.

settling accuracy, which is a significant factor of VPL jitter impact.

## V. Conclusions

In this paper we have presented an analysis of the performance of a new jitter suppressing SC topology. A theoretical background to the different delay line imperfections has been presented and the results have been verified through simulations. The importance of jitter preservation has been discussed and how it influences the performance of the proposed sampler. This paper has been a theoretical study and practical experiments have to be made in order to determine if jitter is preserved, and to what extent, when passing through delay elements.

The delay line is the base of the sampler topology and for suppression to be maximized it is crucial to design a jitter-tolerant delay-line using a fully differential architecture. If the delay jitter is higher than about 30% of the clock jitter, no suppression is achieved, given the parameters chosen in this paper. Also, inband suppression is not

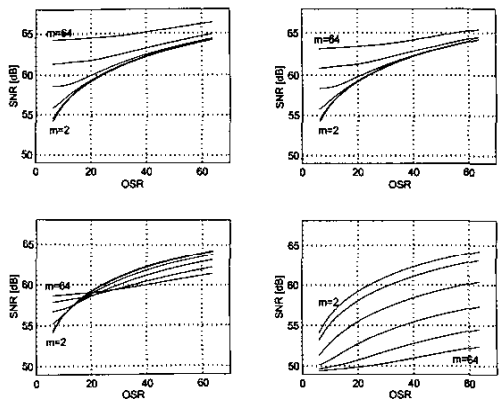


Fig. 6. Plot of inband SNR when varying the OSR for $f_s$ = 96 MHz, $f_{\text{sig}}$ = 750 kHz. $m = \{2, 4, 8, 16, 32, 64\}$, $\sigma_d = \{0.01, 0.1, 0.3, 1\}\sigma_{\text{NUS}}$, and $\sigma_{\text{NUS}} = \frac{0.1}{f_s}$.

as high as $10\log(m)$ dB, which is the case when jitter is not preserved. However, Nyquist range NUS jitter SNR improves as $10\log(m)$ dB. Figure 6 shows a plot of SNR versus OSR for a fix sampling frequency and signal frequency and clearly shows that the proposed sampler topology is best suited for wideband operation. This is because the sampler topology has a higher level of suppression farther away from the signal.

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